Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

Claims 1-14 (canceled)

Claim 15 (previously presented): A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a source electrode;

a drain electrode formed at least in part on the semiconductor layer;

a passivation layer formed on the data line and the drain electrode and having a first contact hole exposing the drain electrode at least in part and a portion of an upper surface of the gate insulating layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole.

Claim 16 (previously presented): The thin film transistor array panel of claim 15, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo, or Mo alloy and an upper film of Al or Al alloy.

Claim 17 (previously presented): The thin film transistor array panel of claim 15, wherein the gate insulating layer comprises silicon nitride and the passivation layer comprises silicon nitride.

Claim 18 (previously presented): The thin film transistor array panel of claim 15, wherein the pixel electrode comprises IZO.

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Claim 19 (previously presented): The thin film transistor array panel of claim 15, wherein the passivation layer has second and third contact holes exposing end portions of the

gate line and the data line, and the thin film transistor array panel further comprises contact assistants contacting the exposed end portions of the gate line and the data line.

Claims 20-24 (canceled)

Claim 25 (previously presented): A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a source electrode;

a drain electrode formed at least in part on the semiconductor layer;

a passivation layer formed on the data line and the drain electrode and having a first contact hole exposing the drain electrode at least in part and a portion of the gate insulating layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole, wherein the pixel electrode contacts an upper surface of the gate insulating layer.

Claim 26 (previously presented): The thin film transistor array panel of claim 25, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo, or Mo alloy and an upper film of Al or Al alloy.

Claim 27 (previously presented): The thin film transistor array panel of claim 25, wherein the gate insulating layer comprises silicon nitride and the passivation layer comprises silicon nitride.

Claim 28 (previously presented): The thin film transistor array panel of claim 25, wherein the pixel electrode comprises IZO.

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Claim 29 (previously presented): The thin film transistor array panel of claim 25, wherein the passivation layer has second and third contact holes exposing end portions of the

gate line and the data line, and the thin film transistor array panel further comprises contact assistants contacting the exposed end portions of the gate line and the data line.

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